Features

- Layered LDPC decoder for 802.11n/ac supporting all code sizes (648, 1296, 1944) and code rates (1/2, 2/3, 3/4, 5/6).
- Supports all 11n MCS classes, 20/40MHz channels and 400/800ns GI with data-rates to 600Mbps (720Mbps coded).
- Supports 11ac classes to 866Mbps with a single decoder at 240MHz and 1.7Gbps at 480MHz.
- Efficient algorithms for high performance
    - corrected or offset min-sum algorithm
    - scaling to prevent bit-growth.
- Integrated handling of puncturing, shortening and repetitions.
- High bandwidth IO with buffering to allow decode during IO.
- Configurable input bit-width.
- Pipelining options to support speed/area trade-off allowing optimal implementation on both ASIC and FPGA.

Deliverables

- RTL (VHDL|Verilog) block description and test harness with test vector files.
- C model and Octave/Matlab sim environment for generation of performance data and RTL verification vectors.
- Performance (BLER/BER/PER) data.
- User Guide and HW Integration Guide.

General Description

The LDPC decoder receives samples from the QAM demapper. The number of input samples read per clock-cycle may be varied from packet to packet, typically as a function of the number of bits in the QAM symbols. The best performance is obtained by positioning the mean level of the demapped bits at a point that offers the best balance between clipping and quantisation. The decoder automatically handles shortening, puncturing and combining of repetitions.

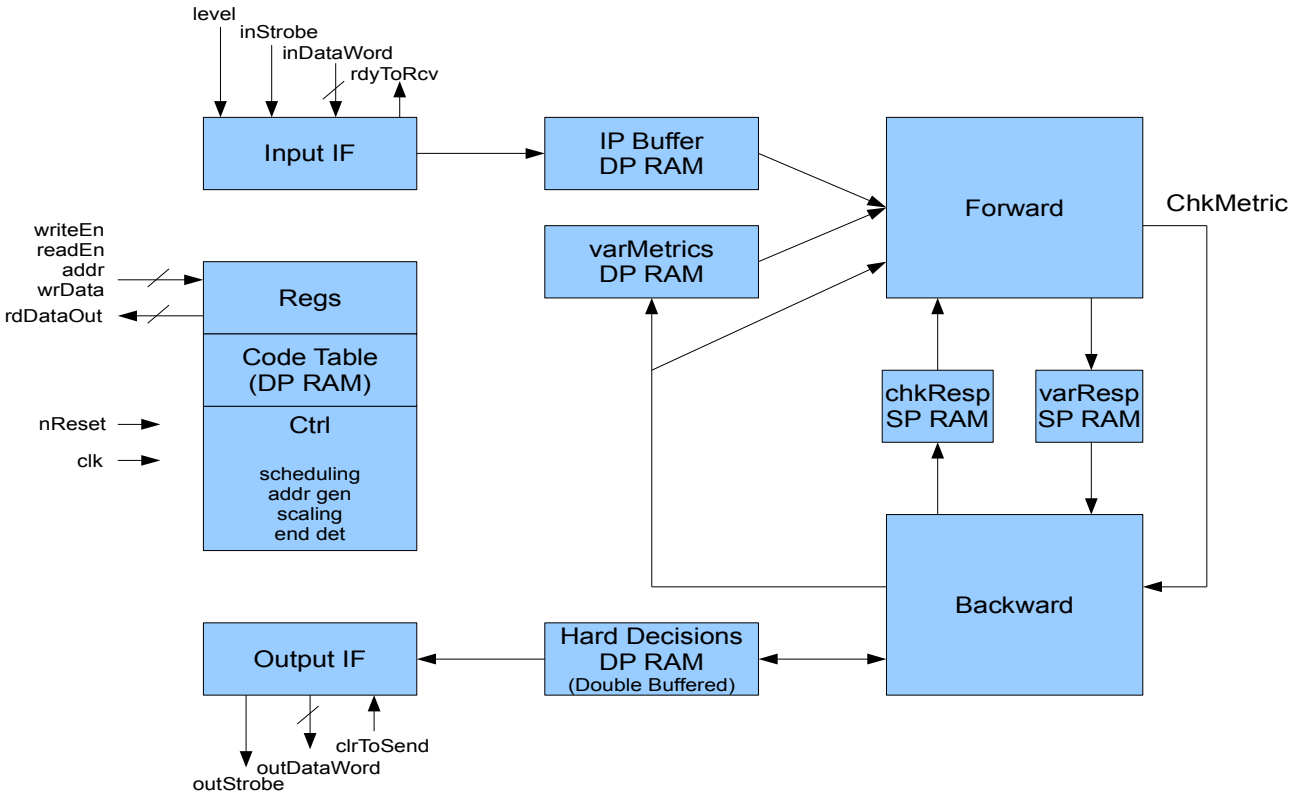
The decoder operates on Z (27, 54, or 81) bits in parallel to process one code macro cell per clock cycle. The code description is programmed at the start of a packet and consists of around 88 macro cells definitions organised in rows. A complete decode iteration therefore takes around 88 clock cycles but in the first iteration there is also a 'priming' delay due to the fact that the backward section lags the forward section by one row.

The forward and backward sections run in synchronisation but with a one row offset. The forward section 'accumulates' a check metric for the row and the backward section then uses this to create check responses and variable metrics. Each variable is 'used' several times in the code table so a complete iteration results in several updates of the variable metric, and a check response for each cell. The size of the variable metrics memory is the code size (Z*24 words) and the check response memory is around Z*88 words.

The check response is the key element of the decode algorithm. When a bit is used in a parity check equation it is possible to calculate its probable value based on the estimates of the other bits used in that equation. The check metric is just an intermediate number needed in the calculation of the check response.

Check metrics and responses are calculated using variable estimates called variable responses. For any given cell the variable response is the relevant variable metric with the check response subtracted out to ensure indepedence. Clearly variable estimates can be calculated on the-fly and we do this in the forward section to create the check metric, however the data is also needed in the backward section to generate the check response (chkMetric - varResp) and so the required information is passed with a FIFO. In slower applications the FIFO would not be needed, but 802.11n is very demanding and the memory fetches of the source information would imply extra memory ports.

The block diagram illustrates the processing blocks and memories. Most layered LDPC decoder's are likely to appear similar at this high level, however most of the design effort is the refinement of the min-sum corrections, scaling method and scheduling strategies to produce an economic design that also performs well.



Performance

Typical implementation losses are 0.2 - 0.4dB compared to a near perfect reference. This low loss is comprised of the following elements:

1. Finite precision arithmetic. The recommended configuration results in approximately a 0.1dB loss.
2. The corrected min-sum approximation. This performs to approximately 0.1dB of the true mathematics that uses exponentials. Note that the un-corrected min-sum approximation would have resulted in a loss of greater than 0.5dB.
3. Limited number of iterations. A 240MHz clock ensures good performance to 600Mbps with losses of 0.1-0.2dB compared to 50 iterations, which has near perfect performance.

For more formal and extensive performance data please ask for the detailed specification.

Maturity and Verification

This design has been targetted to ASIC and FPGA technology by customers with applications ranging from 802.11ac to proprietary (i.e. non-WiFi) wide-area broadband.

In addition we have our own FPGA implementation that verifies functionality and measures performance across multiple MCS and with varying packet lengths (including 1MB for 11ac).

Customisation

The decoder design is flexible and has the potential to be used for applications other than 802.11n/ac subject to contract. Please contact us with your requirements.

Licence

The licence is tiered to allow migration from a development licence to single or multiple use manufacturing licences. Support and Maintenance will be provided for 12 months in the form of clarifications about the product and bug-fixing as well as design enhancements.

The licence provides access to the technical information of the product and does not imply a licence from parties that may claim ownership of the technology, for example through patents. You will certainly need to investigate *Essential IPR* licensing requirements before making an 802.11n product.

Full terms and conditions are provided with formal quotations.

Warranty

This deliverable provides an 802.11n/ac LDPC decoder that may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Any functional or performance defects preventing 802.11n qualification will be resolved inside and outside of the maintenance period.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets. The simplest product choice is to take only the RTL, however if you wish additional flexibility and the rights to modify the design then you can take the algorithm product as well.

Code	Description	
LDPCENC11NR	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR*	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR	802.11ad LDPC Encoder RTL IP	
LDPCDECADR	802.11ad LDPC Decoder RTL IP	
VITDEC11NR	802.11n/ac Viterbi Decoder RTL IP	
AESCRYPTO	AES Cryptography with CCM, and (optionally) CMAC and GCM.	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with 30 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk .