Features

- Supports all 802.11n/ac code sizes (648, 1296, 1944) and rates (1/2, 2/3, 3/4, 5/6).
- Automatic insertion of shortening bits, puncturing of parity bits and generation of repetition bits.
- Multi-user contexts and arbitration.
- Simple software control – configured once at the start of the packet.
- Very high speed encode rate. Z (27, 54, or 81) bits are encoded in parallel.
- Configurable IO bit-widths.
- Total encode times of 2.1uS (16 bit Input, 8 bit output) and 1.52uS (16 bit input and output), with a 240MHz clock. Optional double buffering reduces encode time to 1.2uS (16 bit Input, 8 bit output).
- Efficient hardware architecture. Approximately 20K ASIC gates and 2997 bits of single port RAM.

Deliverables

- RTL (VHDL) block description and test harness with test vector files.
- C model.
- User and Hardware Integration Guides.

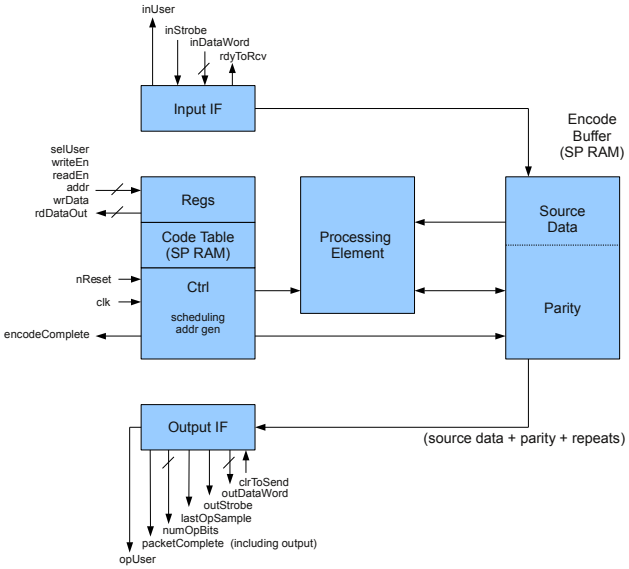
General Description

This product provides low latency, high throughput encoding of 802.11n packets. Configuration by software is only required once per packet. The block autonomously loads a block of input data, encodes it and then delivers it to downstream hardware.

A small memory stores data, while a single, high bandwidth, processing element (PE) performs the necessary syndrome and parity generation, stepping through each code 'macro cell' at a rate of around 2 cycles per cell.

The encode time is extremely low and IO overheads dominate the overall latency. Even then, the IO bandwidth is configurable so that the encode latency can easily be reduced to a small proportion of the overall system latency budget thus easing the constraints on other blocks.

Block Diagram



Implementation Notes

As a rough guide, an ASIC implementation of this IP is estimated to contain around 20K gates of logic and two RAM instances totalling 2997 bits. The RAM is single port and write-maskable features are required (or are emulated by separating the encoder RAM into several slices).

The RTL has been targetted at Xilinx XC6 FPGAs and operating speeds as high as 240MHz have been seen. Typically the design would be operated on a clock shared with other blocks, and the speed will be determined by the slowest of these. We envision a 150MHz clock on an FPGA, with the encoder's IO increased to 16 bit to maintain the bandwidth.

Licence

The licence will allow use of the RTL so that you can make and sell a physical end product ,such as FPGA or ASIC, but you may not re-sell or otherwise disclose the LDPC encoder IP. The contract is tiered to allow migration from a development licence, to single, double then multiple uses up to 10. Support and Maintenance will be provided for 6 months in the form of clarifications about the product and bug-fixing as well as design enhancements.

The licence provides access to the technical information of the product and does not imply a licence from parties that may claim ownership of the technology, for example through patents. You will certainly need to investigate *Essential IPR* licensing requirements before making an 802.11n product.

See the full licence agreement for further details.

Warranty

This deliverable claims to provide an 802.11n LDPC encoder that may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Any functional or performance defects preventing 802.11n qualification will be resolved inside and outside of the maintenance period.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets. The simplest product choice is to take only the RTL, however if you wish additional flexibility and the rights to modify the design then you can take the algorithm product as well.

Code	Description	
LDPCENC11NR*	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR	802.11ad LDPC Encoder RTL IP	
LDPCDECADR	802.11ad LDPC Decoder RTL IP	
VITDEC11NR	802.11n/ac Viterbi Decoder RTL IP	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with more than 25 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk