Features

- Supports all 802.11ad code rates (1/2, 5/8, 3/4, 13/16).
- Automatic insertion of shortening bits and generation of repetition bits.
- Simple control – configured once at the start of the packet with enable, code rate and repeat mode signals.
- 3.2, 4.4, 5.8, 6.6 Gbps encode rate for each code rate respectively, assuming 250MHz clock.
- The top 11ad class (MCS 24) is supportable using a 300MHz clock.
- Configurable IO bit-widths using optional IO interface blocks.
- Efficient hardware architecture. Approximately 20K ASIC gates for the core plus 5-15K for the optional IO interface blocks (depending on configuration).

Deliverables

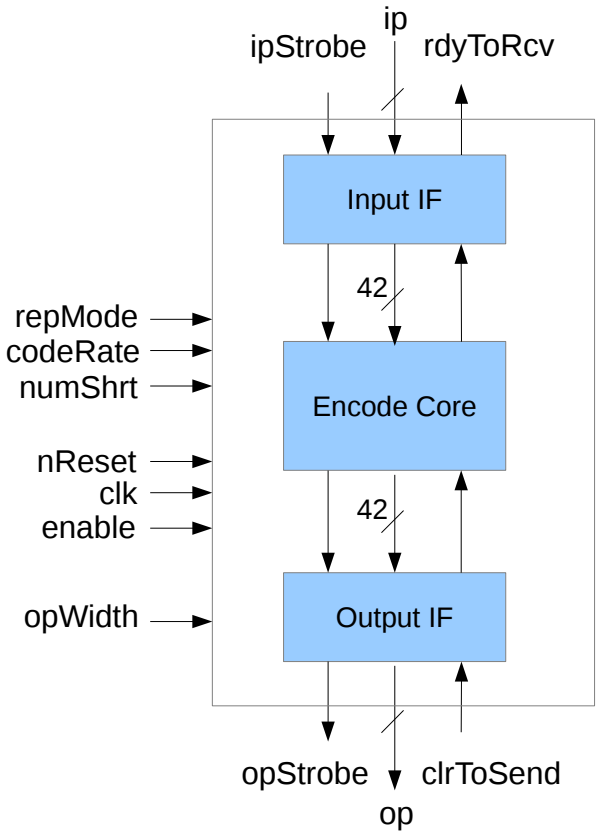
- RTL (VHDL) block description and test harness with test vector files.
- C model.
- User Guide and Hardware Integration Guide.

General Description

This product provides low latency and high throughput encoding of 802.11ad packets. Encoding is on-the fly, so input data is streamed through without storage and with only a single cycle of latency in the core. The core operates on 42 bit wide words, which may be adapted to alternative word widths using the optional input and output interface blocks.

The core includes a repetition buffer for MCS 1 support and supports shortening, which is required for MCS 1 and the control PHY.

Block Diagram



Licence

The licence will allow use of the RTL so that you can make and sell a physical end product, such as an FPGA or ASIC, but you may not re-sell or otherwise disclose the LDPC encoder IP. The contract is tiered to allow migration from a development licence, to single or multiple chip manufacturing licences. Support and Maintenance will be provided for 12 months in the form of clarifications about the product and bug-fixing as well as design enhancements.

The licence provides access to the technical information of the product and does not imply a licence from parties that may claim ownership of the technology, for example through patents. You will certainly need to investigate *Essential IP* licensing requirements before making an 802.11ad product.

See the full licence agreement for further details.

Warranty

This deliverable claims to provide an 802.11ad LDPC encoder that may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Any functional or performance defects preventing 802.11ad qualification will be resolved inside and outside of the maintenance period.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets.

Code	Description	
LDPCENC11NR	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR*	802.11ad LDPC Encoder RTL IP	
LDPCDECADR	802.11ad LDPC Decoder RTL IP	
VITDEC11NR	802.11n/ac Viterbi Decoder RTL IP	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with more than 25 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk