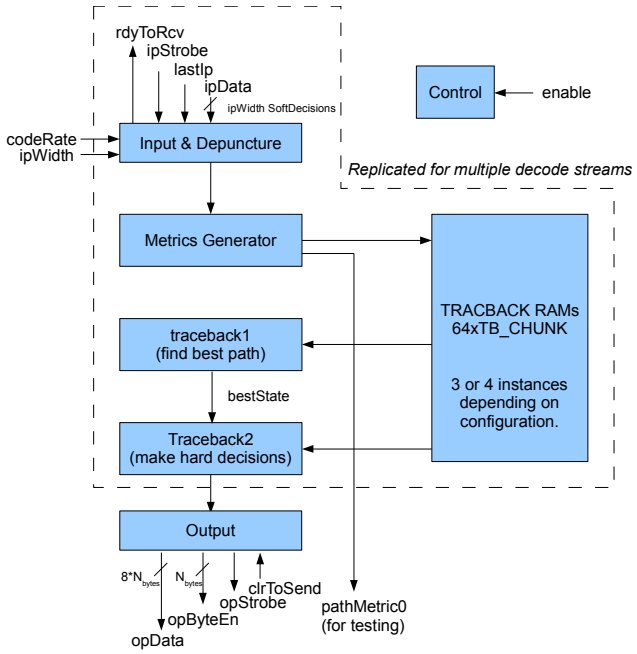
Features

- Supports all 11n/ac MCS classes when configured appropriately.
- Continuous stream decoding.
- Configurable number of decoded bits per cycle (typically 2 or 3 for WiFi).
- Multiple decode streams (multiple logical decoders).
- Puncturing support to alllow 1/2, 2/3, 3/4, 5/6 code rates.
- Input interface supporting:
    - programmable number of input LLRs.
    - insertion of de-puncturing bits.
- Output interface supporting:
    - round-robin merging of multiple-decode streams.
    - formation of output byte streams (configurable width).
- RTL (Verilog) block description and test harness with test vector files.
- C model and Octave/Matlab sim environment for generation of performance data and RTL verification vectors.
- Performance (BLER/BER) data.
- User Guide and HW Integration Guide.



General Description

This block uses the well known Viterbi algorithm to decode 802.11n/ac convolutional coded data. The algorithm is inherently sequential and, in its simplest form, delivers one decoded bit per cycle. 802.11n/ac, however needs higher throughput, which is achieved in two ways:

1. The standard splits higher rate MCS into multiple decoding streams. The IP may be configured to support multiple streams. Multiple decoders are synthesised internally and their output is correctly interleaved as per the standard.
2. Each decoding stream in 802.11n/ac may be up to 585MBPS. To support this throughput the decoder may be configured to generate multiple output bits per cycle. 2 bits/cycle are needed with a clock rate of over 293MHz, while 3 bits/cycle are needed with a clock rate in the range 195-292MHz.

Unlike some other standards, the convolutionally coded stream in 802.11n/ac is continous and could, for example, be 1MB long. This is handled by processing the stream continuously. The Viterbi traceback procedure is carried out concurrently with the continued reception of further data. Once the traceback output has started it will continuously deliver N decoded bits per cycle (where N is configurable).

There are two stages to traceback for a stream decoder. The first traces back from the latest bit with the objective of converging on the best trellis state and then a further traceback is performed to decode the data. The tracebacks are performed periodically on chunks of data. If the chunk size is TB_CHUNK then delay until first output bit is 2 TB_CHUNK bits.

The continuously decoded bits are periodically transferred to an output block where they are formed into bytes. The output interface may be configured to output multiple bytes (1, 2 or 4 being the most common). Where multiple decoder streams have been configured, the output of each stream is taken in round-robin order.

Performance

Typical implementation losses are 0.1-0.2dB with 5-bit input LLRs. This assumes 256 QAM operation.

For more formal and extensive performance data please ask for the detailed specification.

Maturity and Verification

This is a new design verified only in simulation.

Customisation

The decoder design is flexible and has the potential to be used for applications other than 802.11n/ac subject to contract. Please contact us with your requirements.

Licence

Licencing is split into development and manufacturing licences.

Full terms and conditions are provided with formal quotations.

Warranty

This deliverable provides an 802.11n/ac Viterbi decoder that may be practically implemented on an FPGA or ASIC assuming high performance parts or processes. Any functional or performance defects preventing 802.11n/ac qualification will be resolved inside and outside of the maintenance period.

Product Selector

The following table shows this product (highlighted with *) alongside related products. Click the PDF icon to view the datasheets. The simplest product choice is to take only the RTL, however if you wish additional flexibility and the rights to modify the design then you can take the algorithm product as well.

Code	Description	
LDPCENC11NR	802.11n/ac LDPC Encoder RTL IP	
LDPCDEC11NR	802.11n/ac LDPC Decoder RTL IP	
LDPCENCADR	802.11ad LDPC Encoder RTL IP	
LDPCDECADR	802.11ad LDPC Decoder RTL IP	
VITDEC11NR*	802.11n/ac Viterbi Decoder RTL IP	
AESCRYPTO	AES Cryptography with CCM, and (optionally) CMAC and GCM.	

About Blue Rum Consulting

Blue Rum Consulting is a UK limited company offering the services and products of Michael Rumsey, a Wireless ASIC engineer with 30 years of experience. You can find him on linked-in and the company web-site at www.bluerum.co.uk .